INTERPOLATION FILTER STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 90115215, filed June 22, 2001.

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to an interpolation filter. More particularly, the present invention relates to an interpolation filter that utilizes a microprocessor to generate interpolation signals.

Description of Related Art

[0002] Multi-rate filters are widely adopted inside digital audio systems such as compact disks and digital audio tape players. These filters convert a set of input samples into another set of data, which represents the sampling of identical analogue signals at different rates. The two principal implementations of a multi-rate filter are decimation and interpolation. In the interpolation, existing data are computed to increase sampling rate and fill in the missing data between signal samples.

[0003] The process of converting from a discrete-time signal to a continuous-time signal is called a reconstruction. The interpolation method can be regarded as a reconstruction from another discrete-time signal to a continuous-time signal. The reconstruction of continuous-time (analogue) signal and the reconstruction of the

discrete-time (digital) signal are both processes of turning the same into analogue signal. Fig. 1 is a diagram showing a conventional method of reconstructing a continuous-time signal. As shown in Fig. 1, the continuous discrete-time signal x(n) consists of an impulse train. The amplitude of this impulse train corresponds to the sample x(n) at time nT. In practice, this type of conversion is actually implemented by a digital/analogue converter and the results of the conversion are a continuous signal y(t). To smooth out the continuous signal y(t) and produce a reconstructed analogue signal $x_c(t)$, a low-pass reconstruction filter is often used.

[0004] Fig. 2 is a diagram showing the discrete-time signal obtained by a conventional interpolation method. As shown in Fig. 2, the discrete-time signal x(n) is a multiple of L=4. Within the discrete-time signal x(n) are L-1 zero value sampling points. A signal w(m) is obtained by inserting these zero value points. A smooth signal y(m) is derived after passing the signal w(m) through a low-pass filter. Since one x(n) sample corresponds to L y(m) samples, the sampling rate increases L times.

[0005] The interpolation low-pass filter has a finite impulse response (FIR) structure (alternatively, an infinite impulse response (IIR) structure). The signal y(m) computed by the convolution equation of a filter is as follows:

$$y(m) = \sum_{k=0}^{N-1} h(k)w(m-k);$$

where h(k) an impulse function, N-1 is the number of filter coefficient in the impulse function h(k), w(m-k) is an expansion formula according to an input signal x(n) ratio, and the relationship between the signal w(m-k) and the signal x(n) is given by:

w(m-k) = x(m-k)/L when m = k = $0,\pm L,\pm 2L,\ldots$; and

w(m-k) = 0, for others.

[0006] Fig. 3 is a block diagram showing the internal architecture of a conventional interpolation filter. As shown in Fig. 3, the function of an FIR filter (or an IIR filter) is implemented using a microprocessor 302 (in Fig. 3, the microprocessor is labeled ADSP-2100) and its associated assembly language. When the IRQ terminal of the microprocessor 302 receives a signal from a timer 304, the microprocessor 302 executes to filter an input discrete-time signal submitted from an analogue/digital converter 306. Furthermore, the microprocessor 302 uses a software program (for example, such as the one shown in Fig. 4) to produce the interpolation signal having the desired sampling rate. Finally, the interpolation signal is transmitted to a latching circuit 308.

[0007] The microprocessor must hold the filter coefficient and the input signal in order to carry out any interpolation filter function. Moreover, the microprocessor must compute the interpolation signal according to the sampling rate. If the sampling rate is high, time required for calculating the interpolation signal is longer. Because both data transfer and signal computation use up some microprocessor's processing time (in other words, instruction cycles), other tasks are forced to slow down.

SUMMARY OF THE INVENTION

[0008] Accordingly, one object of the present invention is to provide an interpolation filter structure that uses neighboring input discrete-time signals to generate interpolation signals having a desired sampling rate without any data transfer and signal calculation by a microprocessor. Hence, some microprocessor instruction cycles are saved.

[0009] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides an interpolation filter structure. The structure includes a first gain multiplexer, a second gain multiplexer, an adder and a multiplexer. The first gain multiplexer receives a control signal, a previous discrete-time signal and a current discrete-time signal. The first gain multiplexer selects the previous discrete-time signal or the current discrete-time signal according to the control signal and performs a multiplication computation with a first gain value to produce a first gain signal. The second gain multiplexer receives a control signal, a previous discrete-time signal and a current discrete-time signal. The second gain multiplexer selects the previous discrete-time signal or the current discrete-time signal according to the control signal and performs a multiplication computation with a second gain value to produce a second gain signal. The adder adds together the first gain signal and the second gain signal to produce an add signal. The multiplexer receives the control signal, the previous discrete-time signal and the add signal. According to the control signal, the previous discrete-time signal or the add signal is selected to serve as a discrete-time interpolation signal.

[0010] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The

drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0011] Fig. 1 is a diagram showing a conventional method of reconstructing a continuous-time signal;

[0012] Fig. 2 is a diagram showing the discrete-time signal obtained by a conventional interpolation method.

[0013] Fig. 3 is a block diagram showing the internal architecture of a conventional interpolation filter;

[0014] Fig. 4 is a program listing showing steps for operating a conventional interpolation filter;

[0015] Fig. 5 is a block diagram showing the internal architecture of an interpolation filter according to this invention; and

[0016] Fig. 6 is a diagram showing the discrete-time signals after interpolation according to this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0018] The interpolation filter of this embodiment completes a total of three interpolation calculations within a system clocking cycle. Before conducting an interpolation calculation, the sampling signal is a discrete-time signal X[n] that has a sampling rate of Fs. After an interpolation calculation, the sampling signal is a discrete-

time signal Y[n] that has a sampling rate of Fs'. The sampling rates Fs and Fs' are related by Fs' = 3*Fs'. Furthermore, the discrete-time signal X[n] and the discrete-time signal Y[n] are related by the following equations:

$$Y[3k] = X[k-1];$$

$$Y[3k+1] = 0.75*X[k-1]+0.25*X[k];$$

$$Y[3k+2] = 0.75*X[k]+0.25*X[k-1]$$

where k is an integer.

[0019] Fig. 5 is a block diagram showing the internal architecture of an interpolation filter according to this invention. The system implements the mathematical function between the aforementioned discrete-time signals X[n] and Y[n] so that a multi-rate filter is produced. The system includes a first gain multiplexer 514, a second gain multiplexer 516, an adder 510 and a multiplexer 512. In Fig. 5, a counter (not part of the interpolation filter, hence not shown) produces the necessary control signal CNT. The control signal CNT provided by the counter (not shown) has a sampling cycle of 1/Fs. The counter starts counting from 1 to 2 to 3 and then back again to one in cycles.

[0020] The first gain multiplexer 514 comprises a multiplexer 502 and a gain unit 504. Similarly, the second gain multiplexer 516 comprises a multiplexer 506 and a gain unit 508. The input terminals of the multiplexer 502 receive the discrete-time signals X[k-1] and X[k], respectively. If the control signal CNT received by the multiplexer 502 is one, the multiplexer 502 outputs the discrete-time signal X[k-1] to serve as a signal M1. On the other hand, if the control signal CNT received by the multiplexer 502 is two, the multiplexer 502 output the discrete-time signal X[k] to serve as the signal M1. The gain unit 504 picks up the signal M1 from the multiplexer 502 and multiplies the signal M1 by

a gain value to produce a gain signal S1. Thereafter, the gain signal S1 is transmitted from the gain unit 504 to the adder 510. Here, the gain value is 0.75.

[0021] The input terminals of the multiplexer 506 receive the discrete-time signals X[k-1] and X[k], respectively. If the control signal CNT received by the multiplexer 506 is one, the multiplexer 506 outputs the discrete-time signal X[k] to serve as a signal M2. On the other hand, if the control signal CNT received by the multiplexer 506 is two, the multiplexer 506 output the discrete-time signal X[k-1] to serve as the signal M2. The gain unit 508 picks up the signal M2 from the multiplexer 506 and multiplies the signal M2 by a gain value to produce a gain signal S2. Thereafter, the gain signal S2 is transmitted from the gain unit 508 to the adder 510. Here, the gain value is 0.25.

[0022] The adder 510 performs an addition of the gain signal S1 submitted by the gain unit 504 and the gain signal S2 submitted by the gain unit 508 to produce an add signal (ADD). The ADD signal is transmitted from the adder 510 to the multiplexer 512. One input terminal of the multiplexer 512 receives the ADD signal from the adder 510 while the other input terminal of the multiplexer 512 receives the discrete-time signal X[k-1]. If the multiplexer 512 receives a control signal CNT equal to 1 or 2, the multiplexer 512 outputs the ADD signal. The output ADD signal is the interpolation discrete-time signal Y[n]. If the multiplexer 512 receives a control signal CNT equal to 3, the multiplexer 512 outputs a discrete-time signal X[k-1]. The output discrete-time signal X[k-1] is the interpolation discrete-time signal Y[n].

[0023] Consequently, the relationship between the aforementioned discrete-time signal X[n] and interpolation discrete-time signal Y[n] can be summarized as:

$$Y[n] = Y[3k] = X[k-1] \text{ when CNT} = 3;$$

$Y[n] = Y[3k+1] = 0.75*X[k-1]+0.25*X[k]$ when CNT = 1;

$Y[n] = Y[3k+2] = 0.75*X[k]+0.25*X[k-1]$ when CNT = 2

[0024] Hence, according to the hardware structure shown in Fig. 5, three interpolated results are obtained, namely: Y[3k], Y[3k+1] and Y[3k+2]. Fig. 6 is a diagram showing the discrete-time signals after interpolation according to this invention.

[0025] In conclusion, this invention provides an interpolation filter structure that uses neighboring input discrete-time signals to generate interpolation signals having a desired sampling rate without any data transfer and signal calculation by a microprocessor. Hence, some microprocessor instruction cycles are saved.

[0026] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.